

What is claimed is:

1. A field effect transistor comprising:  
an insulating vanadium dioxide thin film used as a channel material;  
a source electrode and a drain electrode disposed on the insulating vanadium  
5 dioxide thin film to be spaced apart from each other by a channel length;  
a dielectric layer disposed on the source electrode, the drain electrode, and  
the insulating vanadium dioxide thin film; and  
a gate electrode for applying a predetermined voltage to the dielectric layer.

10 2. The field effect transistor of claim 1, wherein the vanadium dioxide thin  
film is disposed on a silicon substrate, a silicon-on-insulator substrate, or a sapphire  
substrate.

15 3. The field effect transistor of claim 1, wherein the dielectric layer is  
selected from the group consisting of  $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$  ( $0 \leq x \leq 0.6$ ),  $\text{Pb}_{1-x}\text{Zr}_x\text{TiO}_3$  ( $0 \leq x \leq 0.5$ ),  
 $\text{Ta}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{SiO}_2$ .

20 4. The field effect transistor of claim 1, wherein the source electrode, the  
drain electrode, and the gate electrode are gold/chromium electrodes.

25 5. A method of manufacturing a field effect transistor, comprising:  
forming a vanadium dioxide thin film on a substrate;  
forming a source electrode and a drain electrode on the vanadium dioxide thin  
film to cover portions at both right and left sides of the vanadium dioxide thin film;  
forming a dielectric layer on the substrate, the source electrode, the drain  
electrode, and the vanadium dioxide thin film; and  
forming a gate electrode on the dielectric layer.

30 6. The method of claim 5, wherein the substrate is selected from the  
group consisting of a single crystal silicon substrate, a silicon-on-insulator substrate,  
and a sapphire substrate.

7. The method of claim 5, further comprising patterning the vanadium

dioxide thin film to have an area of several  $\mu\text{m}^2$ .

8. The method of claim 7, wherein the patterning is performed using a photolithography process and a radio frequency-ion milling process.

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9. The method of claim 5, wherein the source electrode, the drain electrode, and the gate electrode are formed using a lift-off process.